UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/885,290	06/19/2001	Thomas Markson	55218-0519	3062

29989 7590 12/17/2004

HICKMAN PALERMO TRUONG & BECKER, LLP
1600 WILLOW STREET
SAN JOSE, CA 95125

EXAMINER	
TODD, GREGORY G	

ART UNIT	PAPER NUMBER
2157	

DATE MAILED: 12/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/885,290	MARKSON ET AL.	
	Examiner	Art Unit	
	Gregory G Todd	2157	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/09/02,01/30/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is a first office action in response to application filed, with the above serial number, on 19 June 2001 in which claims 1-39 are presented for examination. Claims 1-39 are therefore pending in the application.

Oath/Declaration

2. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because:
The signatures are not dated.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 13 and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. There are no "third instructions" to give basis for "fourth instructions".

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Pothapragada et al (hereinafter "Pothapragada", 6,389,432).

As per Claim 1, Pothapragada teaches a method of selectively allocating storage to a processor comprising the computer-implemented steps of:

receiving a request to allocate storage to the processor (at least col. 2, lines 4-38; col. 7, lines 19-55; request for storage space); and

configuring a virtual storage layer to logically associate one or more logical units from among one or more storage units to the processor (at least col. 2, lines 4-38; col. 7, lines 19-55; allocated and assigning LUN).

As per Claim 2. A method as recited in claim 1, wherein the configuring step is carried out without modification to an operating system of the processor (at least col. 2, lines 4-38; col. 7, lines 19-55).

As per Claim 3. A method as recited in claim 1, wherein the configuring step is carried out by a control processor that is coupled through one or more storage networks to a plurality of storage gateways that are coupled through the storage networks to the one or more storage units (at least col. 2, lines 4-38; col. 3 line 66 - col. 4 line 39; Fig. 1; controller, server, fibre channel switch).

As per Claim 4. A method as recited in claim 1, wherein the configuring step further comprises the steps of:

configuring a storage gateway in the virtual storage layer to map the logical units to a boot port of the processor (at least col. 2, lines 4-38; col. 7, lines 19-55; request for storage space); and

configuring the one or more storage units to give the processor access to the logical units (at least col. 2, lines 4-38; col. 7, lines 19-55; request for storage space).

6. Claims 1-10, 14-17, and 21-39 are rejected under 35 U.S.C. 102(e) as being anticipated by Blumenau et al (hereinafter "Blumenau", 6,421,711).

As per Claim 1, Blumenau teaches a method of selectively allocating storage to a processor comprising the computer-implemented steps of:

receiving a request to allocate storage to the processor (at least col. 31, lines 27-39; col. 33, lines 29-66; host requesting allocation of a volume); and

configuring a virtual storage layer to logically associate one or more logical units from among one or more storage units to the processor (at least col. 31, lines 9-51; col. 33 line 53 - col. 34 line 50; allocated and assigning LUN).

As per Claim 2. A method as recited in claim 1, wherein the configuring step is carried out without modification to an operating system of the processor (at least col. 31, lines 9-51; col. 33 line 53 - col. 34 line 50).

As per Claim 3. A method as recited in claim 1, wherein the configuring step is carried out by a control processor that is coupled through one or more storage networks to a plurality of storage gateways that are coupled through the storage networks to the one or more storage units (at least col. 11, lines 3-30; Fig. 1; col. 31, lines 9-61, gatekeeper and fibre channel switch).

As per Claim 4. A method as recited in claim 1, wherein the configuring step further comprises the steps of:

configuring a storage gateway in the virtual storage layer to map the logical units to a boot port of the processor (at least col. 32 line 13 - col. 33 line 17; boot from storage subsystem volume); and

configuring the one or more storage units to give the processor access to the logical units (at least col. 31, lines 9-51).

As per Claim 5. A method as recited in claim 1, wherein the virtual storage layer comprises a control processor that is coupled through a storage network to a storage gateway, wherein the storage gateway is coupled through the storage network to the one or more storage units, and wherein the configuring step further comprises the steps of:

the control processor issuing instructions to the storage gateway to map the logical units to a boot port of the processor (at least col. 32 line 13 - col. 33 line 17; boot from storage subsystem volume); and

the control processor issuing instructions to the storage units to give the processor access to the one or more logical units (at least col. 31, lines 9-51).

As per Claim 6. A method as recited in claim 1, wherein the configuring step further comprises the steps of:

receiving the request to allocate storage at a control processor that is coupled through a storage network to a storage gateway, wherein the storage gateway is coupled through the storage networks to the one or more storage units (at least col. 11, lines 3-30; Fig. 1; col. 31, lines 9-61, gatekeeper and fibre channel switch);

instructing the storage gateway to map the one or more logical units to a boot port of the processor (at least col. 32 line 13 - col. 33 line 17; boot from storage subsystem volume); and

instructing the one or more storage units to give the processor access to the one or more logical units (at least col. 31, lines 9-51).

As per Claim 7. A method as recited in claim 1, wherein:

the method further comprises the step of storing first information that associates processors to logical units, and second information that associates logical units to storage units (at least col. 21 line 16 - col. 22 line 21; host to LUN to logical volume), and

the configuring step further comprises the step of mapping the one or more logical units from among the one or more storage units to a boot port of the processor

by reconfiguring the virtual storage layer to logically couple the one or more logical units to the boot port based on the stored first information and second information (at least col. 32 line 13 - col. 33 line 17; boot from storage subsystem volume).

As per Claim 8. A method as recited in claim 1, further comprising the step of generating the request to allocate storage at a control processor that is communicatively coupled to a control database, wherein the request is directed from the control processor to a storage manager that is communicatively coupled to the control processor, the control database, and a storage network that includes a disk gateway (at least col. 11, lines 3-30; Fig. 1; col. 31, lines 9-61; col. 29 line 58 - col. 30 line 12; gatekeeper and fibre channel switch with configuration database), and

wherein the step of configuring the virtual storage layer includes reconfiguring the disk gateway to logically couple the one or more logical units to a boot port of the processor (at least col. 32 line 13 - col. 33 line 17; boot from storage subsystem volume).

As per Claim 9. A method as recited in claim 8, further comprising the step of issuing instructions from the storage manager to the one or more storage units to give the processor access to the one or more logical units (at least col. 31, lines 9-51).

As per Claim 10. A method as recited in claim 1, wherein the configuring step further comprises the steps of:

identifying one or more logical units (LUNs) of the one or more storage units that have a sufficient amount of storage to satisfy the request (at least col. 32 line 13 - col. 34 line 59; col. 9, lines 44-57);

instructing a storage gateway in the virtual storage layer to map the identified LUNs to the small computer system interface (SCSI) port zero of the processor based on a unique processor identifier (at least col. 32 line 13 - col. 34 line 59; col. 9, lines 44-57); and

instructing the one or more storage units to give the processor having the unique host identifier access to the identified LUNs (at least col. 31, lines 9-51).

As per Claim 14. A method as recited in claim 1, wherein the one or more logical units associated with the processor include at least one logical unit from a first volume from the one or more storage units, and at least one logical unit from a second volume from among the one or more storage units (at least Fig. 19; col. 21, lines 16-67).

As per Claim 15. A method as recited in claim 1, wherein the request to allocate storage specifies an amount of storage to be allocated (at least col. 31 line 9 - col. 32 line 12; col. 6 line 64 - col. 7 line 65; col. 9, lines 44-57; col. 32, lines 58-67; col. 34, lines 2-17).

As per Claim 16. A method as recited in claim 1, wherein the request to allocate storage specifies a type of storage to be allocated (at least col. 31 line 9 - col. 32 line 12; col. 6 line 64 - col. 7 line 65; col. 9, lines 44-57; col. 32, lines 58-67; col. 34, lines 2-17).

As per Claim 17, Blumenau teaches a method of selectively associating storage with a host processor without modification to an operating system of the host, comprising the steps of:

receiving a request to associate the storage at a virtual storage layer that is coupled to a plurality of storage units and to one or more host processors, wherein the request identifies a particular host processor and an amount of requested storage (at least col. 31; lines 9-61);

configuring the virtual storage layer to logically couple one or more logical units from among the plurality of storage units having the requested amount of storage to a standard boot port of the particular host processor, by instructing a storage gateway in the virtual storage layer to map the one or more logical units to the standard boot port of the particular host processor, and instructing the plurality of storage units to give the particular host processor access to the one or more logical units (at least col. 11, lines 3-30; Fig. 1; col. 31, lines 9-61; col. 32 line 13 - col. 33 line 17; boot from storage subsystem volume).

As per Claim 21, Blumenau teaches a method of selectively associating storage with a host processor, comprising the steps of:

receiving, at a virtual storage layer that is coupled to a plurality of storage units and to one or more host processors, a request to associate the storage, wherein the request identifies the host processor and an amount of storage to be associated with the host processor (at least col. 31; lines 9-61);

mapping one or more sub-units of storage from among the plurality of storage units to a standard boot port of the host processor by logically coupling the one or more sub-units to the standard boot port of the host processor by instructing a gateway to couple the host processor to the one or more sub-units and by instructing the plurality of storage units (at least col. 32 line 13 - col. 33 line 17; boot from storage subsystem volume).

As per Claim 22, Blumenau teaches a computer-readable medium carrying one or more sequences of instructions for selectively associating storage with a host processor in a networked computer system, wherein execution of the one or more sequences of instructions by one or more processors causes the one or more processors to perform the steps of:

receiving a request to associate the storage at a virtual storage layer that is coupled to a plurality of storage units and to one or more host processors that have no then-currently assigned storage, wherein the request identifies a particular host and an amount of requested storage (at least col. 31; lines 9-61);

mapping one or more logical units from among the storage units having the requested amount of storage to a standard boot port of the identified host, by reconfiguring the virtual storage layer to logically couple the logical units to the boot port (at least col. 32 line 13 - col. 33 line 17; boot from storage subsystem volume).

As per Claim 23, Blumenau teaches an apparatus for defining and deploying a networked computer system, comprising:

means for receiving a request at a virtual storage layer that is coupled to a plurality of storage units to associate storage with a particular host processor, wherein the request specifies an amount of requested storage (at least col. 31; lines 9-61);

means for mapping one or more logical units from among the plurality of storage units having the amount of requested storage to a standard boot port of the particular host processor by reconfiguring the virtual storage layer to logically couple the one or more logical units to the standard boot port of the particular host processor (at least col. 32 line 13 - col. 33 line 17; boot from storage subsystem volume).

As per Claim 24, Blumenau teaches an apparatus for defining and deploying a networked computer system, comprising:

a processor (at least col. 31; lines 9-61);

a computer-readable medium accessible to the processor and storing a textual representation of a logical configuration of the networked computer system according to a structured markup language (at least col. 31; lines 9-61);

one or more sequences of instructions stored in the computer-readable medium and which, when executed by the processor, cause the processor to carry out the steps of:

receiving a request to associate storage, wherein the request is received at a virtual storage layer that is coupled to a plurality of storage units to a

particular host processor, wherein the request specifies an amount of requested storage (at least col. 31; lines 9-61);

mapping one or more logical units from among the plurality of storage units having the requested amount of storage to a standard boot port of the particular host processor by reconfiguring the virtual storage layer to logically couple the one or more logical units to the boot port of the particular host processor (at least col. 32 line 13 - col. 33 line 17; boot from storage subsystem volume).

As per Claim 25, Blumenau teaches a system for selectively associating storage with a host processor, comprising:

a virtual storage mechanism that is coupled to a plurality of storage units and to one or more host processors (at least col. 31; lines 9-61);

a control processor that is communicatively coupled to the virtual storage mechanism and that comprises a computer-readable medium carrying one or more sequences of instructions which, when executed by one or more processors, cause the one or more processors to carry out the steps of:

receiving a request to associate storage with a particular host processor, wherein the request identifies an amount of requested storage (at least col. 31; lines 9-61);

mapping one or more logical units from among the storage units having the requested amount of storage to a standard boot port of the particular host processor, by reconfiguring the virtual storage mechanism to logically couple the one or more logical units to the standard boot port of the particular host processor (at least col. 32 line 13 - col. 33 line 17; boot from storage subsystem volume).

As per Claim 28. A system as recited in claim 25, wherein the control processor is communicatively coupled to a control database that comprises first information that associates hosts to logical units, and second information that associates logical units to storage units (at least col. 11, lines 3-30; Fig. 1; col. 31, lines 9-61; col. 29 line 58 - col. 30 line 12; gatekeeper and fibre channel switch with configuration database); and

wherein the sequences of instructions of the control processor further comprise instructions which, when executed by the one or more processors, cause the one or more processors to carry out the steps of mapping one or more logical units from among the plurality of storage units having the requested amount of storage to the standard boot port of the particular host processor by reconfiguring the virtual storage mechanism to logically couple the one or more logical units to the standard boot port of the particular host processor based on the first information and the second information (at least col. 32 line 13 - col. 33 line 17; boot from storage subsystem volume).

As per Claim 33, Blumenau teaches a method of selectively allocating storage to a processor comprising the computer-implemented steps of:

receiving a request to allocate storage to the processor (at least col. 31, lines 27-39; col. 33, lines 29-66; host requesting allocation of a volume); and

logically assigning one or more logical units from among one or more storage units to the processor, wherein the one or more logical units include at least one logical unit from a first volume from the one or more storage units and at least one logical unit from a second volume from the one or more storage units (at least Fig. 19; col. 21, lines 16-67).

As per Claim 34. A method as recited in claim 1, wherein the configuring step is carried out by a switch device in a storage area network (at least col. 11, lines 3-30; Fig. 1; col. 31, lines 9-61; col. 41, lines 34-54; SAN and fibre channel switch).

As per Claim 35. A method as recited in claim 1, wherein the configuring step is carried out by a disk array in a storage area network (at least col. 11, lines 3-30; Fig. 1; col. 7, lines 51-65; col. 31, lines 9-61; col. 41, lines 34-54; SAN and RAID).

As per Claim 36. A method as recited in claim 1, wherein the one or more logical units associated with the processor include at least one logical unit comprising a first volume of storage of a first storage unit and a second volume of storage from a second storage unit (at least Fig. 19; col. 21, lines 16-67).

As per Claim 37. A method of selectively allocating storage to a processor comprising the computer-implemented steps of:

receiving a symbolic definition of a virtual server farm that includes a storage definition (at least col. 21 line 16 - col. 22 line 63; LUN - VOL NO) ;

based on the storage definition, creating a request to allocate storage to the processor (at least col. 31, lines 27-39; col. 33, lines 29-66; host requesting allocation of a volume); and

configuring a virtual storage layer to logically associate one or more logical units from among one or more storage units to the processor (at least col. 31, lines 9-51; col. 33 line 53 - col. 34 line 50; allocated and assigning LUN).

As per Claim 38. A method as recited in claim 37, wherein the storage definition identifies an amount of requested storage and a SCSI target for the storage (at least col. 31 line 9 - col. 32 line 12; col. 6 line 64 - col. 7 line 65; col. 9, lines 44-57; col. 32, lines 58-67; col. 34, lines 2-17).

As per Claim 39. A method as recited in claim 37, wherein the storage definition identifies an amount of requested storage and a file system mount point for the storage (at least col. 31 line 9 - col. 32 line 12; col. 6 line 64 - col. 7 line 65; col. 9, lines 44-57; col. 32, lines 58-67; col. 34, lines 2-17).

Claims 26, 27 and 29-32 do not substantially add or define any additional limitations over claims 3, 5, and 10-13 and therefore are rejected for similar reasons.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 11-13 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blumenau in view of Ofer et al (hereinafter "Ofer", 6,260,109).

As per Claim 11. A method as recited in claim 1, wherein the configuring step comprises:

issuing a request to allocate one or more volumes on one of the one or more storage units (at least col. 31, lines 27-39; col. 33 line 29 - col. 34 line 50);

configuring the volume for use with the processor (at least col. 31, lines 9-51);

issuing first instructions to the one or more storage units to bind the processor to the volume by giving the processor access to the volume (at least col. 33 line 29 - col. 34 line 50);

issuing second instructions to a gateway in the virtual storage layer to bind the volume to the processor (at least col. 33 line 29 - col. 34 line 50; eg. gatekeeper).

Blumenau fails to explicitly teach the volume being concatenated. However, the use and advantages for using such concatenation is well known to one skilled in the art at the time the invention was made as evidenced by the teachings of Ofer (at least Abstract). Therefore, it would have been obvious to one of ordinary skill in the art at the

time the invention was made to incorporate Ofer's use of concatenation into Blumenau's system as this would enhance Blumenau's RAID arrays and subsequently allocated logical volumes to be combined together as this is well known in the art in expanding storage.

As per Claim 12. A method as recited in claim 11, further comprising the steps of:

determining that the second instructions have failed to bind the concatenated volume to the processor (at least col. 33 line 29 - col. 34 line 50);

issuing third instructions to the one or more storage units to un-bind the processor from the concatenated volume (at least col. 33 line 29 - col. 34 line 50; removing and deallocating).

Claims 18-20 do not substantially add or define any additional limitations over claims 11-13 and therefore are rejected for similar reasons.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Denning et al, Nguyen et al, Nolan et al ('526, '278), Popelka et al, Hickman et al, Tamer et al, and Blumenau '442 are cited for disclosing pertinent information related to the claimed invention. Applicants are requested to consider the prior art reference for relevant teachings when responding to this office action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gregory G Todd whose telephone number is (571)272-

4011. The examiner can normally be reached on Monday - Friday 9:00am-6:00pm w/ first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ario Etienne can be reached on (571)272-4001. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Gregory Todd
Patent Examiner
Technology Center 2100

SALEH NAJJAR
PRIMARY EXAMINER